REMARKS

The Office Action dated July 23, 2003 has been reviewed and carefully considered. Claims 1-12 remain pending in this application, claim 1 being the independent claim. Reconsideration in view of the following remarks is respectfully requested.

Claims 1-6, 9 and 11-12 stand rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent No. 6,362,094 to Dabbaugh et al. ("Dabbaugh").

35 U.S.C. 102(e) states that "A person shall be entitled to a patent unless –

> (e) the invention was described in - (1) an application for patent, published under **section 122(b)**, by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in **section 351(a)** shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Dabbaugh has an effective filing date of August 16, 2000, whereas the present application has priority dates of March 13, 2000 and May 31, 2000 as seen from the attached first pages of the U.S. patent publication and the corresponding international patent application. The May 9, 2002 Office Action acknowledges the priority claim and receipt of all of the certified copies of the priority documents. Accordingly, the Dabbaugh reference is not prior art with respect to the claims of the present application, and therefore does not anticipate the claims for at least this reason.

The applicants request that a requirement for an English translation of the priority documents be held in abeyance pending prompt preparation of the translations and their submission to the Office.

Claims 7-8 and 10 stand rejected under 35 U.S.C. 103(a) as unpatentable over Dabbaugh in view of Boeck et al. (US 5,888,018).

Dabbaugh likewise does not serve as prior art for an obviousness rejection of claims 7-8 and 10 for at least the same reason discussed above.

Reconsideration and withdrawal of the anticipation and obviousness rejections is respectfully requested.

For all the foregoing reasons, it is respectfully submitted that all the present claims are patentable in view of the cited references. A Notice of Allowance is respectfully requested.

Respectfully submitted,

Aaron Waxler
Registration No. 48,027

Date: 10/23/03

By: Steve Cha
Attorney for Applicant
Registration No. 44,069

Mail all correspondence to:
Aaron Waxler, Registration No. 48,027
US PHILIPS CORPORATION
P.O. Box 3001
Briarcliff Manor, NY 10510-8001
Phone: (914) 333-9608
Fax: (914) 332-0615

Certificate of Mailing Under 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to MAIL STOP NON-FEE AMENDEMENT, COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA. 22313 on 10/23/03.

Steve Cha, Reg. No. 44,069
(Name of Registered Rep.)

(Signature and Date)

US 20010046784A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2001/0046784 A1**

Broekaart et al. (43) **Pub. Date: Nov. 29, 2001**

(54) **METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE**

(76) Inventors: **Marcel Eduard Irene Broekaart**, Nijmegen (NL); **Josephus Franciscus Antonius Maria Guelen**, Nijmegen (NL); **Eric Gerritsen**, Nijmegen (NL)

Correspondence Address:
U.S. Philips Corporation
580 White Plains road
Tarrytown, NY 10591 (US)

(21) Appl. No.: **09/804,004**

(22) Filed: **Mar. 12, 2001**

(30) **Foreign Application Priority Data**

Mar. 13, 2000 (EP) 00201166.6
May 31, 2000 (EP) 00201928.9

Publication Classification

(51) **Int. Cl.**[7] **C30B 1/00**; H01L 21/20; H01L 21/36; H01L 21/4763; H01L 21/302; H01L 21/461

(52) **U.S. Cl.** **438/740**; 438/483; 438/637

(57) **ABSTRACT**

A method of manufacturing an electronic device, a semiconductor device in particular but not exclusively, which method comprises the steps of:

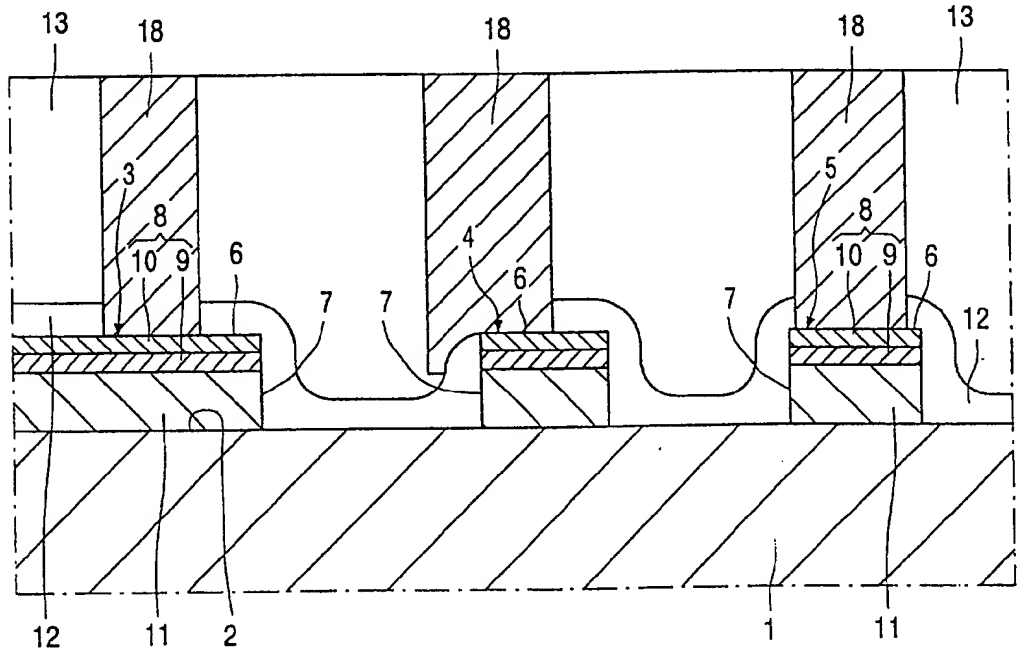
applying a semiconductor substrate (**1**) which is provided with a conductor (**3,4,5**) at a surface (**2**), the conductor (**3,4,5**) having a top surface portion (**6**) and sidewall portions (**7**), of which at least the top surface portion (**6**) is provided with an etch stop layer (**12**) comprising silicon carbide,

applying a dielectric layer (**13**),

etching a via (14,15,16) in the dielectric layer (**13**) over the conductor (**3,4,5**), and stopping on the etch stop layer (**12**) to create an exposed part of the etch stop layer (**12**),

removing the exposed part of the etch stop layer (**12**) inside the via (**14,15,16**) from at least the top surface portion (**6**) of the conductor (**3,4,5**),

filling the via (**14,15,16**) with a conductive material (**18**).



(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
20 September 2001 (20.09.2001)

PCT

(10) International Publication Number
WO 01/69672 A1

(51) International Patent Classification[7]: H01L 21/768, 23/532

(21) International Application Number: PCT/EP01/02431

(22) International Filing Date: 5 March 2001 (05.03.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
00201166.6 13 March 2000 (13.03.2000) EP
00201928.9 31 May 2000 (31.05.2000) EP

(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors: BROEKAART, Marcel, E., I.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). GUELEN, Josephus, F., A., M.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). GERRITSEN, Eric; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: DUIJVESTIJN, Adrianus, J.; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

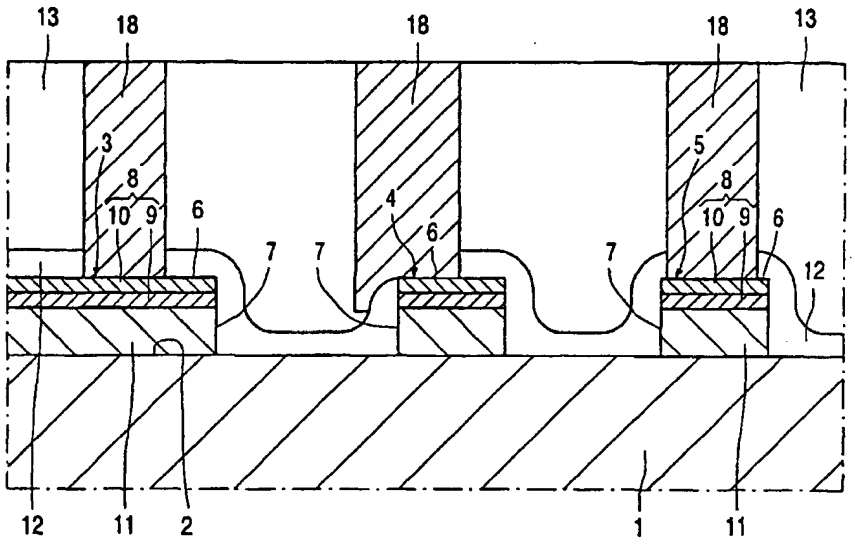
(81) Designated States *(national)*: JP, KR.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: A METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE



(57) Abstract: A method of manufacturing an electronic device, a semiconductor device in particular but not exclusively, which method comprises the steps of: applying a semiconductor substrate (1) which is provided with a conductor (3, 4, 5) at a surface (2), the conductor (3, 4, 5) having a top surface portion (6) and sidewall portions (7), of which at least the top surface portion (6) is provided with an etch stop layer (12) comprising silicon carbide; applying a dielectric layer (13); etching a via (14, 15, 16) in the dielectric layer (13) over the conductor (3, 4, 5), and stopping on the etch stop layer (12) to create an exposed part of the etch stop layer (12); removing the exposed part of the etch stop layer (12) inside the via (14, 15, 16) from at least the top surface portion (6) of the conductor (3, 4, 5); filling the via (14, 15, 16) with a conductive material (18).

WO 01/69672 A1